A Digitally Controlled Solid-State Transformer Architecture for Smart Grid-Oriented Low-Voltage DC Distribution Systems

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***Abstract*—Solid-state transformers (SSTs) have emerged as an alternative to conventional transformers by integrating high-frequency power electronic converters and advanced digital control. This paper presents the design and simulation of a one-kilowatt microcontroller-based solid-state transformer prototype. This SST design consists of a two-stage architecture: an AC-DC boost power factor correction (PFC) circuit and a DC-DC phase-shifted full-bridge (PSFB) circuit. An STM32 microcontroller is employed to execute the PI control algorithm. Simulation studies in PLECS software show a total harmonic distortion (THD) of 3.68 percent in the input current, a power factor of 0.9954, and an output voltage ripple of 2.1 percent. The system achieves an overall efficiency of 93.94 percent. These results confirm that the design complies with industrial power quality standards, offering a highly efficient and flexible solution for smart grids, renewable energy systems, and electric vehicle (EV) charging infrastructures.**

Keywords—Solid-state transformer, power factor correction, phase-shifted full-bridge

I. INTRODUCTION

The increased integration of renewable energy systems, electric vehicles, and smart grid technologies has created a critical need for highly efficient, controllable power conversion architectures [1]-[2]. Conventional transformers operate at low frequencies, which requires massive magnetic components, resulting in heavy structures with limited controllability.

Due to these disadvantages, traditional transformers are not suitable for applications requiring modern power management systems. Developments in the semiconductor field have paved the way for solid-state transformers (SSTs) as an alternative [1], [3]. By integrating high-frequency switching elements, such as MOSFETs and diodes, into advanced power electronics converters, SSTs efficiently perform voltage conversion while providing galvanic isolation [3]-[4]. High-frequency operation significantly reduces the size of magnetic components and increases the power density of the grid infrastructure [4].

Solid-state transformers can provide active voltage regulation, harmonic filtering, reactive power compensation, and bidirectional power flow management within a single system architecture [2]-[3]. These capabilities enable the grid integration of renewable energy sources, such as solar and wind, by actively controlling and mitigating power-quality degradation [2], [5]. Recent reviews further identify the SST as a key enabling technology for resilient and sustainable smart grids and for medium-voltage electric-vehicle (EV) extreme-fast-charging stations, where conventional line-frequency transformers become a bottleneck [2], [6]. In parallel, the growing deployment of microgrids has further intensified the need for controllable converter interfaces and adaptive energy-management strategies [7]-[8].

At the converter level, the boost power-factor-correction (PFC) rectifier remains the preferred AC/DC front-end stage for kilowatt-class applications because of its low input-current harmonics and near-unity power factor [9]. In contrast, the phase-shifted full-bridge (PSFB) topology is widely adopted for the isolated DC/DC stage, since its zero-voltage switching (ZVS) operation reduces switching losses at high frequency [10]. The maturation of low-cost microcontrollers has, in turn, made it practical to implement such multi-loop digital control schemes on a single embedded platform [11].

Several isolated DC/DC converter topologies have been reported for SST applications; among them, the dual-active bridge, LLC resonant converter, and PSFB are the most widely adopted [1]-[3]. Despite their respective advantages, the DAB requires a sophisticated modulation strategy [12], and the LLC demands variable-frequency control for wide load range regulation [13], both increasing implementation complexity. The PSFB was therefore selected, as it achieves ZVS at a fixed switching frequency with relatively simple digital control [10].

In this study, a 1 kW digitally controlled solid-state transformer (SST) prototype was designed and simulated. The proposed architecture features a two-stage topology comprising a power-factor-correction (PFC) AC/DC converter and an isolated DC/DC stage based on a phase-shifted full-bridge (PSFB) converter. Key switching operations are managed by an STM32 microcontroller using tailored pulse width modulation (PWM) schemes to regulate output parameters across varying operating regimes. To ensure grid reliability and compliance with MIL-STD-461G,

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an electromagnetic interference (EMI) filter is integrated into the grid interface. The system offers selectable dual outputs of 24 V and 48 V in both AC and DC modes, providing a flexible platform. Consequently, this work examines the practical implementation constraints of a fully digital SST and validates the performance advantages of advanced power electronics conversion technologies.

II. System Architecture

The proposed SST performs a two-stage power conversion from a 230 V AC, 50 Hz grid input to selectable 24 V or 48 V outputs in both AC and DC form. Fig. 1 illustrates the top-level block diagram of the system.

Stage 1 is an AC/DC PFC Boost Converter that rectifies and boosts the grid voltage to a regulated 360 V DC link while ensuring near-unity power factor. Stage 2 is an isolated PSFB DC/DC Converter that steps down the DC link to the desired output voltage through a high-frequency transformer.

A. EMI Filter

An EMI filter (AC-CW1B-10A) is strategically placed at the input stage to suppress conducted electromagnetic interference generated by high-frequency switching operations effectively. This filtering stage is critical for attenuating both common-mode and differential-mode noise, ensuring strict system compliance with MIL-STD-461G [14] and IEC 61000-3-2 [15] standards while preventing harmonic pollution on the grid side. Furthermore, NTC (Negative Temperature Coefficient) thermistors are integrated at the mains input to strictly limit severe inrush currents during initial power-up. By offering a high initial resistance that naturally decreases as components warm up during steady-state operation, these thermistors provide crucial electrical protection for downstream PFC rectifiers and sensitive switching devices, ultimately enhancing the converter's overall reliability.

B. AC/DC PFC Boost Converter

The first conversion stage consists of a diode full-bridge rectifier followed by a boost PFC converter. The boost inductor value is designed to limit the maximum current ripple. A dual-loop PI control scheme is implemented: an outer voltage loop regulates the 360 V DC bus, and an inner current loop shapes the input current to be sinusoidal and in phase with the grid voltage, achieving near-unity power factor.

Key design equations for the boost inductor (L), RMS inductor current, and output capacitor are derived from standard PFC design methodology [9]. The output capacitor (1360 µF, implemented as 2 x 680 µF, 400 V) is sized to satisfy both hold-up time and output voltage ripple requirements. The complete PLECS simulation model of the PFC stage is shown in Fig. 2.

C. Phase-Shifted Full-Bridge DC/DC Converter

The second stage is an isolated PSFB converter operating at 50 kHz. The high-frequency transformer has a turns ratio of N_p:N_s = 28:4, selected to achieve the target output voltages while accounting for rectifier diode forward voltage drops. Zero-Voltage Switching (ZVS) is achieved for the leading-leg switches, significantly reducing turn-on losses and improving efficiency [10].

The secondary side uses a full-bridge diode rectifier followed by an LC output filter (L_o = 1.215 µH, C_o = 10 µF). The output voltage ripple is maintained below 0.1%, and the inductor current ripple is kept below 9% of the rated output current. The corresponding PSFB converter simulation model is shown in Fig. 3.

An STM32H723ZG microcontroller generates PWM signals for both the PFC and PSFB stages. The PFC control implements a dual-loop PI scheme with a soft-start to limit

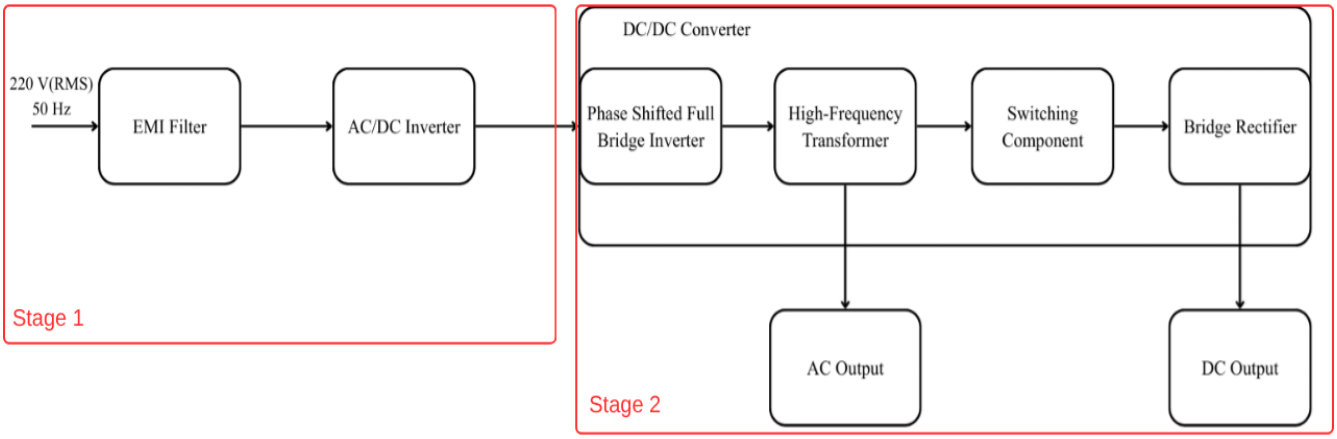

Fig. 1. Top-level block diagram of the system.

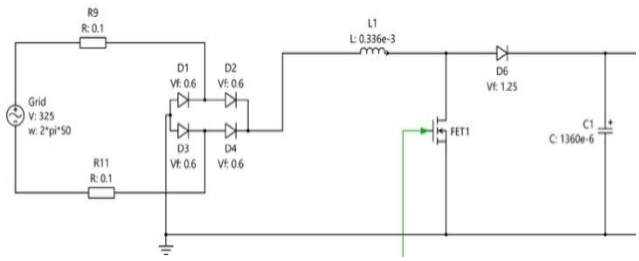

Fig. 2. PFC simulation design

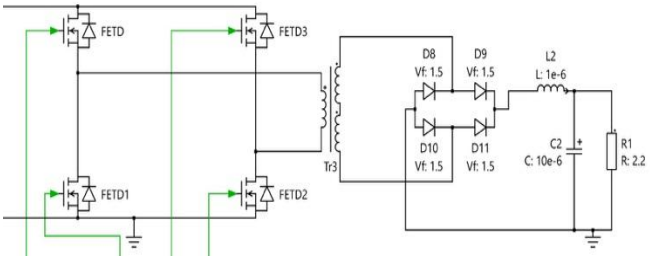

Fig. 3. PSFB simulation design

inrush current. The PSFB stage uses phase-shift modulation to regulate the output voltage. Hall-effect current sensors and an I2C LCD provide real-time monitoring of system parameters.

D. Digital Control Implementation

The proposed solid-state transformer is governed by a centralized digital control platform based on the STM32H723ZG microcontroller. The overall control architecture of the proposed system is illustrated in Fig. 4. To ensure high power quality and grid compliance at the AC/DC PFC boost converter stage, an average current-mode control strategy is implemented using a dual-loop Proportional-Integral (PI) architecture. The control loops are structured as follows:

Outer Voltage Loop: The actual DC output voltage is continuously monitored and compared against a soft-started reference voltage. The resulting error is processed by the primary PI controller to maintain a steady 360 V DC link. A saturation block is actively employed to limit the maximum current demand, thereby ensuring component safety during transient conditions.

Current Reference Shaping: To achieve active power factor correction, the control signal generated by the voltage loop is multiplied by the rectified input voltage signal ($|V_{in}|$). This multiplication ensures the reference current remains strictly in phase with the grid voltage, guaranteeing near-unity power factor operation.

Inner Current Loop: This high-speed loop compares the measured inductor current with the shaped sinusoidal reference. A secondary PI controller minimizes tracking errors, which is highly critical for reducing the total harmonic distortion (THD) and improving overall power quality.

PWM Modulation: Finally, the output of the inner current loop serves as the modulating signal, which is compared against a high-frequency triangular carrier wave to generate the necessary PWM signals. This logic dynamically adjusts the boost MOSFET's duty cycle to regulate energy transfer under variable load conditions.

Furthermore, for the isolated DC/DC PSFB stage, the microcontroller utilizes phase-shift modulation to precisely step down the high-frequency AC voltage and regulate the output to the selectable 24 V or 48 V DC levels.

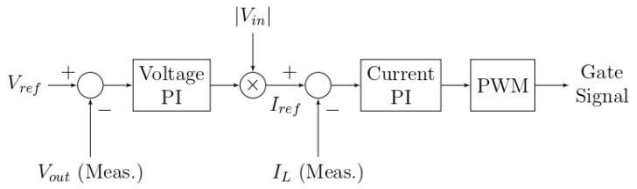

Fig. 4. Digital control architecture of the PFC stage.

III. Mathematical Analysis

A. PFC Stage Design

The boost inductor value is determined from the maximum current ripple constraint. For a 1 kW output at $V_{in,rms}$ = 230 V and $V_{out} \approx$ 360 V, the switching frequency is f_s = 100 kHz:

$$L = \frac{V_{\text{in,rms}}^2}{P_{out} \times \Delta I_L \times f_s} \cong 336\ \mu\text{H} \tag{1}$$

The RMS inductor current is approximately equal to the RMS input current: $I_{L,rms} = P_{out} / V_{in,rms} = 1000/230 \approx 4.35$ A. The copper loss in the inductor winding is $P_{Cu} = I_{L,rms}^2 \times R_{winding} \approx 2.65$ W.

The minimum output capacitance is determined from the hold-up time requirement (t_{hold} = 10 ms): $C_o \geqslant 2 \times P_{out} \times t_{hold} / (V_{out}^2 - V_{min}^2) \approx 965$ µF. A value of 1360 µF is selected to also satisfy the voltage ripple constraint.

B. PSFB Stage Design

The transformer turns ratio is selected as N_p:N_s = 28:4. The secondary voltage and effective phase shift for a 48 V output are:

$$V_S = V_{dc} \times \frac{N_s}{N_p} = 355 \frac{4}{28} \cong 50.71\ \text{V} \tag{2}$$

$$\eta_{eff} = \frac{V_{out} + 2V_f}{V_S} \frac{N_p}{N_s} \cong 0.954 = 95.4\% \tag{3}$$

The maximum flux density in the ETD-54 core is $B_{max} = V_{dc} \times \eta_{eff} / (2 \times N_p \times A_e \times f_s) \approx 0.165$ T, which is within the safe operating range for the selected core material. The total MOSFET switching losses are estimated at approximately 18.7 W for the PSFB stage under worst-case conditions.

IV. Results and Discussion

A. PFC Stage Performance

PLECS simulation results confirm that the PFC stage successfully regulates the DC link at 360.48 V with a voltage ripple of 2.1%, well below the 5% design target, as shown in Fig. 5. The input current waveform is sinusoidal and in phase with the grid voltage, yielding a power factor of 0.9954 and a THD of 3.68% for the first 50 harmonics (Fig. 6). Both values satisfy the IEC 61000-3-2 and IEEE 519-2022 harmonic standards [15]-[16]. The PFC stage reaches steady state without significant overshoot in approximately 0.8 s.

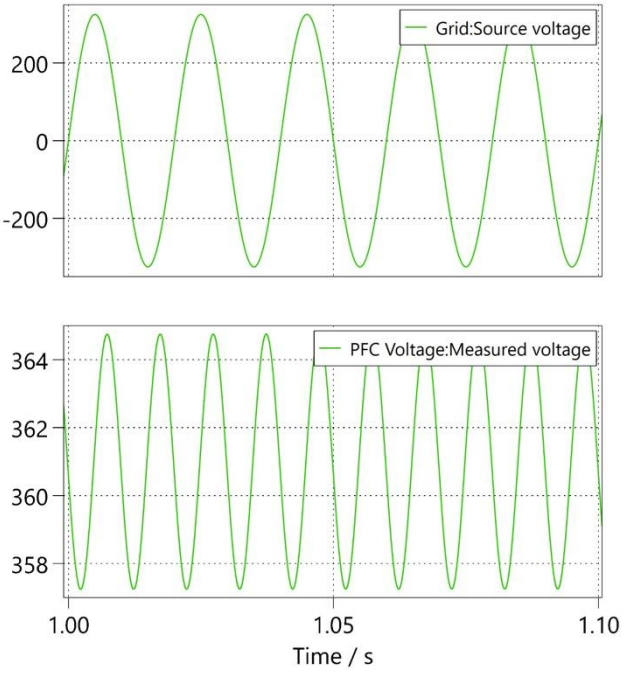

Fig. 5. PFC stage input and output voltage waveforms (V_{IN} and V_{Out}).

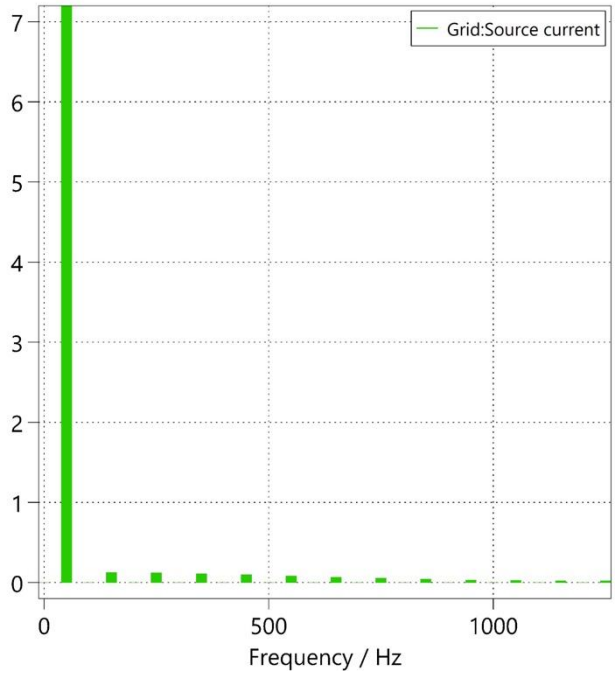

Fig. 6. Input current Fourier spectrum (THD = 3.68%).

B. PSFB DC/DC Stage Performance

The PSFB converter delivers a regulated 48 V output with approximately 23 A of current and 1094.87 W of output power; the corresponding output voltage and current waveforms for the 48 V mode are shown in Fig. 7. In this mode, the output voltage ripple is 0.1% and the settling time is approximately 1.0 s. The output voltage and current waveforms for the 24 V output mode are shown in Fig. 8. The PSFB efficiency is 99.16%, thanks to near-ZVS operation of the leading-leg switches.

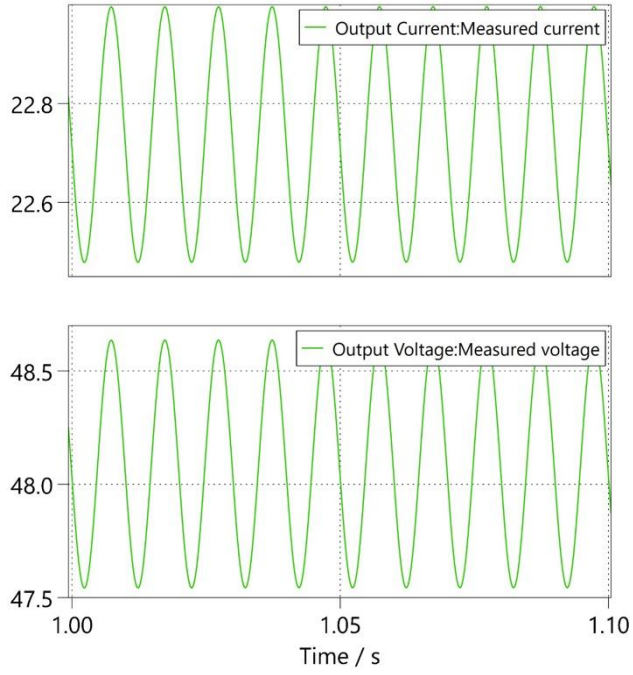

Fig. 7. Output voltage and current of 48 V mode (I_{Out} and V_{Out}).

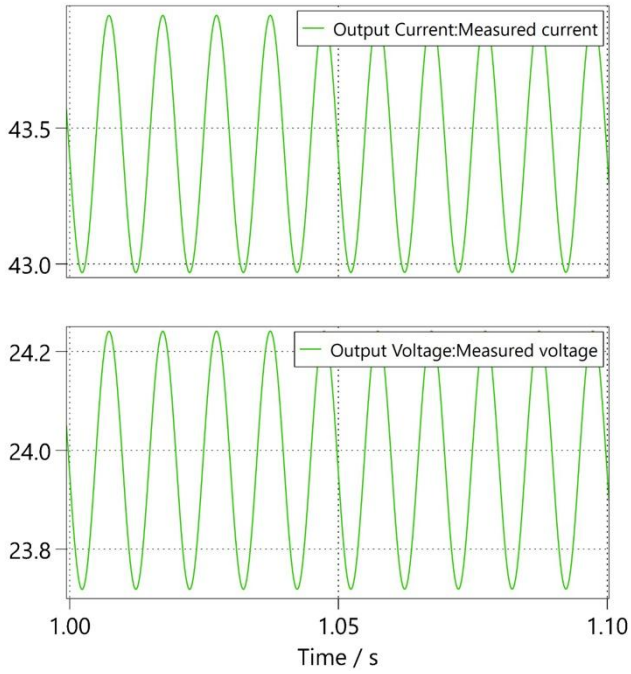

Fig. 8. Output voltage and current of 24 V mode (I_{Out} and V_{Out}).

C. Final System Performance

The combined system achieves a total efficiency of 93.94% at rated load, as summarized by the overall performance characteristics in Fig. 9. Table I summarizes the performance against design targets.

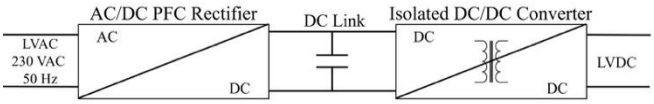

Fig. 9. Final system performance characteristics.

TABLE I. FINAL VALIDATION OF DESIGN PARAMETERS

Parameter	Requirement	Simulation Result
Input Voltage	230 V_{AC}, 50 Hz	230 V_{AC}, 50 Hz
Output Power	1 kW	1094 W
DC-Link Voltage	Approximately 360 V	360.48 V
Power Factor	> 0.99	0.9954
Input Current THD	< 5%	3.68%
PFC Efficiency	> 90%	94.73%
PSFB Efficiency	> 95%	99.16%
Total Efficiency	> 90%	93.94%
Voltage Ripple	< 5%	2.1%
Galvanic Isolation	Required	Transformer-based
Settling Time	< 1.5 s	~1.0 s

The design adheres to multiple industrial and regulatory standards. The PFC control achieves a THD of 3.68%, satisfying the 5% limit mandated by IEC 61000-3-2 and IEEE 519-2022 for harmonic pollution [15]-[16]. An EMI filter designed per MIL-STD-461G is integrated at the input stage [14]. PCB layout follows IPC-2221B guidelines for trace spacing, thermal management, and dielectric strength [17]. All components are RoHS-compliant, restricting the use of hazardous substances in accordance with EU Directive 2015/863 [18].

Electrical safety is ensured by a 25 A fuse for overcurrent protection and a high-frequency transformer that provides 4 kV galvanic isolation. The system is designed for an ambient operating temperature range of 0°C to 50°C, with semiconductor junction temperatures maintained below 130°C under rated operation. An STM32-managed hybrid cooling strategy uses a continuously running fan supplemented by additional fans that activate based on real-time thermal sensor data. The simulation results confirm that all design targets are met. The high PSFB efficiency of 99.16% is primarily due to near-ZVS operation of the leading-leg switches; actual hardware measurements are expected to be slightly lower, due to parasitic elements and gate-driver propagation delays that are not fully captured in the simulation model.

V. Conclusions

This paper presents the design and PLECS simulation of a 1 kW STM32-based Solid-State Transformer for low-voltage DC smart-grid distribution. The proposed two-stage architecture, comprising a PFC boost rectifier and a PSFB isolated DC/DC converter, was evaluated against defined performance targets. Simulation results confirm that the PFC stage achieves a power factor of 0.9954 and an input current THD of 3.68%, satisfying the limits set by IEC 61000-3-2 and IEEE 519-2022 [15]-[16]. The PSFB stage delivers a regulated 48 V output with an efficiency of 99.16%, primarily attributed to near-ZVS operation of the leading-leg switches. The combined two-stage system achieves a total efficiency of 93.94% at rated load, with a DC-link voltage of 360.48 V and an output voltage ripple of 2.1%. These results confirm that all design targets are met. The system complies with MIL-STD-461G [14], IEC 61000-3-2 [15], IEEE 519-2022 [16], IPC-2221B [17], and RoHS standards [18], confirming its suitability for deployment in regulated power environments. The results demonstrate that the proposed SST architecture offers a compact, intelligent, and grid-compatible alternative to conventional transformers, with strong potential for applications in renewable energy integration, EV charging stations, and DC smart grid infrastructure.

Future work will pursue three primary directions. First, hardware prototyping and experimental characterization will be conducted to validate simulation results and quantify the impact of parasitic elements and gate-driver delays on converter efficiency and output quality. Second, the architecture will be extended to support bidirectional power flow, enabling vehicle-to-grid (V2G) operation and facilitating the integration of energy storage in DC microgrids. Since the present prototype relies on unidirectional diode-bridge rectifiers in both the PFC front-end and the PSFB secondary, this extension will require replacing them with active (synchronous) rectifiers and adopting an inherently bidirectional isolated topology such as a dual-active-bridge (DAB) converter. Third, a digital communication interface compliant with IEC 61850 or Modbus will be integrated to enable real-time monitoring, supervisory control, and coordination within smart grid management systems. These developments are expected to advance the readiness of SST technology for large-scale deployment in next-generation power distribution networks.

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